IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

6/C TURNER 10/23/91

Applicant: Gordon E. Morrison et al

Group Art Unit: 237

Serial No. 560,093

Examiner: E. Chan

Filed: July 30, 1990

Title: Parallel Processing Method and Apparatus for Increasing Processing Throughput by Parallel Processing Low Level Instructions Having Natural Concurrencies"

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

10/24/91

AMENDMENT

In response to the Office Action mailed June 4, 1991, please amend the application as follows.

In the Claims

Cancel claims 69 and 70.

Amend claims 71, 72, and 74-83 as follows:

71. (Amended) A system for executing branches in single entry-single [exist] exit (SESE) basic blocks (BBs) contained within a program, each basic block having a plurality of non-branch instructions and ending with a branch instruction, said system comprising:

means [(620)] receptive of said program for determining the branch instruction within each said basic block of said program, said determining means [being] further [capable of] adding firing time information [(IFT)] to said branch instruction,